**Educational Objective:**

The objective of this lab is to gain a better understanding of JFET transfer characteristic and biasing. Important concepts reinforced in this lab include: 1) JFET characteristics in the saturation region, 2) changing PSpice parameters, 3) use of MultiSim for simulation and 4) voltage divider bias design.

**Pre-Laboratory:**

1. In Section 1 transistor equations used by both PSpice and class are given. The PSpice equation uses terms like LAMBDA, BETA and VTO. We will not use LAMBDA so it can be set to zero. Determine BETA and VTO in terms of VP and IDSS by comparing Equation 1, 2 and 3. Put simply, what are BETA and VTO in terms of the more common VP and IDSS?
2. *The Transistor*:

Sketch the JFET transfer characteristics in Figure 1 when VP = -2V and IDSS = 15mA.

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| JFET Transfer Characteristic |

Figure 1

**Overview:**

The lab will introduce you to MultiSim and have you study the transfer characteristics of a JFET. The characteristic curve describes the relationship between Vgs and Id when the JFET is in the saturation region.

**Procedure:**

1. Complete the quiz handed out in lab. The quiz will only be available for the first ten (10) minutes of your laboratory session. The content of this quiz is based on the knowledge you should have gained while completing the pre-lab section of this laboratory activity. You may use your pre-lab as a reference while taking the quiz.

Section 1: Simulate the transfer characteristic curve.

*Use the MultiSim Simulator to graph the JFET’s transfer characteristic curve*

* 1. Open MultiSim.

NOTE: Engineers are constantly faced with the challenge of using new software tools. Not only do they need to teach themselves how to use the new tools, the technicians that work for them will look you for help with the new tool. Engineering tools, unlike most modern software, tends to be complicated and actually need instructions. Fortunately most vendors realize this and provide the needed help document.

* 1. Enter the schematic in figure 2 (and save the design using the instructions below.
     + Open the Getting Started under the Help menu.
     + Read the instructions on schematic capture. Read the placing components and wiring the design.

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| JFET Circuit for Simulating the Transfer Characteristics |

Figure 2

* + - Select “Component” in the Place Menu. Change the group selection from “All Groups” to “transistors”. Find and place the 2N5484.
    - Select “Component” in the Place Menu again. Change the group selection to “Sources” and the family: to “Power Sources”. Find and place the DC\_Power (twice) and Ground.
    - Wire the design so it looks like Figure 2. Double clicking on a component lets you change what is displayed.
      1. Using the Display tab select “Use component-specific visibility settings”
      2. Using the Label tab change the reference designator so it is the same as the figure.
    - Double check the schematic to insure there is a dot where the source, ground and two power supply grounds come together. A common error is to have the wires just cross and not connect so make sure there is a dot.
  1. Changing the PSpice model parameters.

Note: Unfortunately the MultiSim library does not have the U1898 JFET. Fortunately we can change the PSpice model of the 2N5484 so it matches the U1898 (or lab JFET). A few of the most important specifications for the U1898 are show in Figure 3 below. Gate-Source Cutoff Voltage or Vgs(off) is Vp and Zero-Gate Voltage Drain Current is IDSS. The PSpice equation for drain current is:

Equation 1

The class equation is:

Equation 2

The class equation made to look like the PSpice equation to help with prelab:

Equation 3

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| JFET U1898 specifications |

Figure 3

* + - Double click on the JFET and select the Value tab.
    - Click on Edit Model and the PSpice model will be displayed.
    - Delete all parameters from Lambda down just leaving VTO and BETA. Set VTO and BETA using the equation from pre-lab and Vp = -2V and Idss = 15mA.

Caution: BETA is milli. Make sure you enter 3.75E-003.

* + - Click Change Component and OK to close the remaining window.
  1. Sweeping a DC power supply to generate the transfer characteristics.

Note: By varying Vgs and measuring Id the simulation will automatically generate the transfer characteristics.

* + - Select the “Analyses and Simulation” from the Simulation menu.
    - Select “DC Sweep” parameter tab and then select Vgg1 under Sources in source 1.
    - Enter -2V as the start value (this is Vp), enter 0V as the stop value and 0.1 as the increment.
    - Select the Output tab and then Add expression… found in the center of the window.
    - Create –I(VDD) and then press OK.

Note: The letter after the minus sign is I (eye) not 1 (one).

* + - Click Run on the bottom of the window.
    - Double click on the y-axis and the minimum range to 0.
    - Click on the General tab and turn on the grid.
    - Verify Vp and Idss on the plot and make a print for the report.
    - Get a sign-off. Sign-off sheet at the end of the lab.

Section 2: Simulate JFET circuit (Self Bias).

1. *Use the ModelSim Simulator to view the operating point.*
   1. Create the circuit in Figure 4. Double click on each component and change the settings so the values show and the names are correct.
   2. Add the voltage probe and current probes (green buttons at top of screen). Measure: VD, VS and ID. Subtract VD from VS to get VDS.
   3. Make sure the VTO and BETA values are the same as in Section 1.
   4. Select Run (green play button).

Note: If a simulation window pops up a previous simulation setup may still be present. With simulation turned off select “Analyses and Simulation” from the Simulate menu. Select “Interactive Simulation” and then press the “Reset to default” button. Click save to exit.

* 1. Verify VDS is around 14.7V and ID is around 4.3mA.

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| JFET Circuit – Self Bias |

Figure 4

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| JFET Voltage Divider Bias |

Figure 5

Section 3: Design a Voltage Divider Bias.

*Choose RD and RS in Figure 5*Figure 2 *so that IDQ = 2mA and VDSQ = 8V.Let Vp = -2V and Idss = 15mA. The steps below will help.*

1. Use the voltage divider equation to determine Vg. Hints:
   * + Ig = 0
     + The voltage divider equation is Ohm’s Law twice. First find the total current in R1 and R2 (Ohm’s Law once). Then find the voltage across R2 (Ohm’s Law again). If you put the previous two steps into one step you have the “Voltage Divider Equation”.
     + The voltage across R2 is Vg!
2. Use Shockley’s equation and IDQ to determine VGSQ.
3. To find Rs you need the voltage across it (Vs) and the current through it (IDQ). Once these are know you simply use Ohm’s Law. Hints:
   * + Differential voltages like Vgs (two letters subscript) can always be related to node voltages like Vg and Vs (single letter subscript) using the equation. Vgs = Vg - Vs.
     + Remember Vgs is negative so Vs will be larger than Vg.
4. Finally a KVL equation on the right side of Figure 5 will provide Rd.

*Simulate to verify your design*

1. Start MultiSim and enter the schematic in Figure 5 using the values you just determined and the 2N5484 JFET.
2. Change VTO and BETA to make the transistor have a Vp = -2V and Idss = 15mA. Set LAMBDA to zero.
3. Add Multimeters to measure IDQ and VDSQ (the Multimeter is in the Instruments under the Simulate Menu).
4. Simulate the circuit and verify IDQ and VDSQ. The following gives some common errors:
   1. Remember, current must be measured in series.
   2. Forgetting to add VDS (the power supply).
   3. Entering the transistors parameters (VTO and BETA) incorrectly.
5. Obtain a sign-off (end of the lab).
6. *Sign-offs Name*

Section 1: simulated transfer characteristics.

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Section 3: Voltage Divider Bias Circuit

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1. *Post Lab Work*:

Provide a summary, all sign-offs, and the transferred characteristic curve.